

**APPLICATION NOTE**

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**THE OVERSHOOT OF CERAMIC CAPACITOR****Introduction**

Generally Speaking, the power input  $V_{DD}$  pin of IC is usually parallel connected by a ceramic capacitor to ground. If this pin connects power source like wall adapter or USB port via a longer cable, double typical voltage value may import to the input pin of IC as power source turns on. The IC could be destroyed, even burned down. The following detailed description put the cause of this undesirable result in discussion.

**Detailed Description**

In actual application, the input pin of IC is connected to a wall adapter or USB port with a 3-10 feet cable as shown below in figure 1.

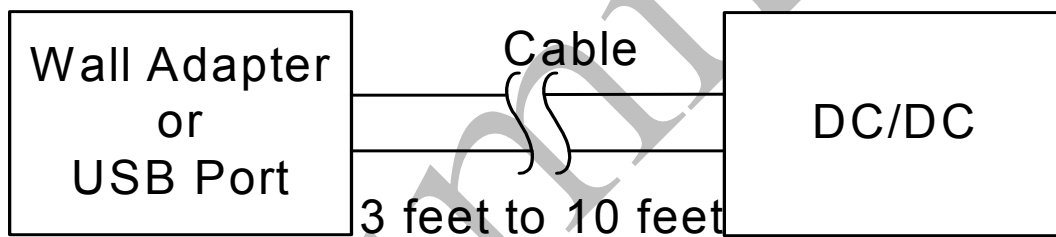


Figure 1

This cable can be modeled as a string of the equivalent inductance  $L_{cb}$  and equivalent resistor  $R_{ind}$ . At the same time, the ceramic capacitor connected in the input pin of IC also has a string of the equivalent inductance  $C_{in}$  and equivalent resistor  $R_{cap}$ . Hence, the overall relationship between the cable and the ceramic capacitor can be represented by a simplified circuit as shown in figure2, where  $V_a$  is the voltage of the wall adapter or USB port and  $V_{in}$  is the voltage of IC's  $V_{DD}$  pin.

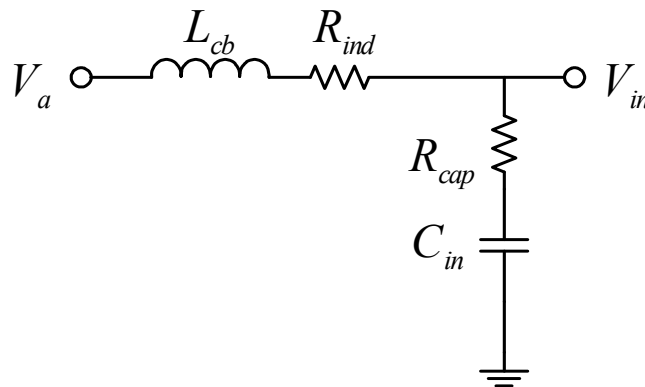
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Figure 2

The transfer function of above model can be described as

$$\frac{V_{in}(s)}{V_a(s)} = \frac{R_{cap}}{L_{cb}} \cdot \frac{s + \frac{1}{C_{in}R_{cap}}}{s^2 + \frac{R_{cap} + R_{ind}}{L_{cb}}s + \frac{1}{L_{cb}C_{in}}} \quad (1)$$

Generally speaking, the equivalent inductance  $L_{cb}$  and equivalent resistor  $R_{ind}$  are small. Hence, these reasonable parameters,  $L_{cb} = 1\mu H$ ,  $R_{ind} = 10m\Omega$ ,  $C_{in} = 22\mu F$ ,  $R_{cap} = 0.01\Omega$  &  $1.01\Omega$ , are chosen for simulation. The step response of equation (1) is depicted as follows.

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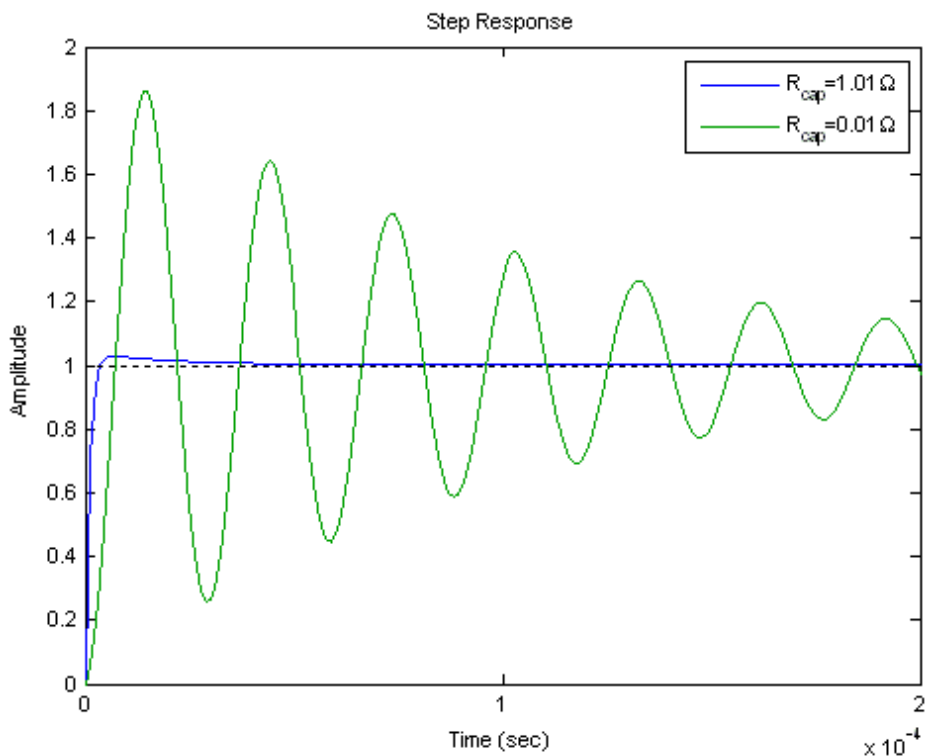


Figure 3

It can be easily observed that the overshoot of this model with  $R_{cap}=0.01\Omega$  is larger than the same model with  $R_{cap}=1.01\Omega$ . However, an equivalent resistor of an ordinary ceramic capacitor is inconveniently  $R_{cap}=0.01\Omega$ . Since this simulation under  $R_{cap}=0.01\Omega$  condition can not be altered, when the voltage of wall adapter or USB port is 5 Volt, the voltage of  $V_{DD}$  pin can increase to up to 9.2 Volt or thereabouts. The IC can not tolerate such high voltage input and can be easily damaged.

**Solution**

Here, a method is proposed to improve high voltage damage risk as shown in figure 4. Using a resistor R equals  $1\Omega$  to be connected to C with series connection can efficiently reduce undesired high voltage. A much safer level of PWR voltage can be adopted to provide guarantee for normal IC operation.



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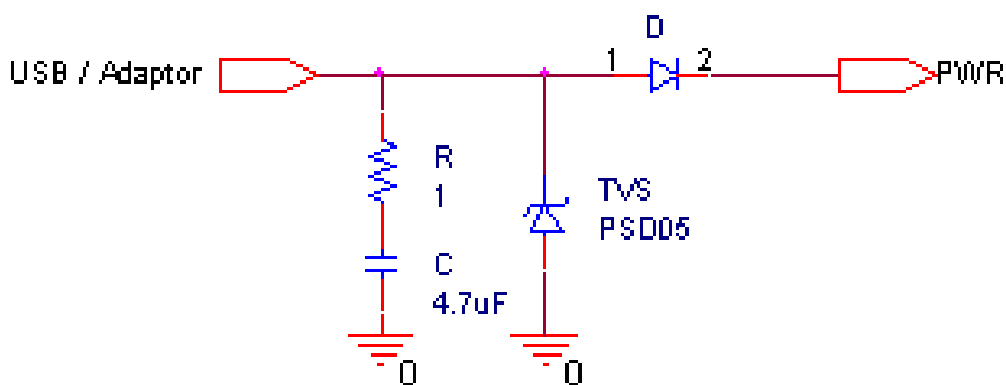


Figure 4

Preliminary